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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/533,807	05/05/2005	Masahiro Nomura	Q87901	8193

23373 7590 08/30/2006

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EXAMINER	
HERNANDEZ, WILLIAM	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 08/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/533,807	NOMURA, MASAHIRO	
	Examiner	Art Unit	
	William Hernandez	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12 and 13* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 May 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20050505*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1-3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 3-2, 103, 104, 110, 111, 112, 1021, 1022, 1023 and 1024.

3. The drawings are objected to because the unlabeled rectangular box(es) shown in Figs. 7, 18, 25, 29, 32 and 38 should be provided with descriptive text labels. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

5. Claims 1-4 and 6-8 are objected to because of the following informalities:

In claims 1-4, the first instance of the phrase "a NOR circuit" should read --a first NOR circuit-- and the second instance should read --a second NOR circuit--.

In claims 6-8, the first instance of the phrase "a NAND circuit" should read --a first NAND circuit-- and the second instance should read --a second NAND circuit--.

In claim 12, the first instance of the phrase "a plurality of PMOSs" should read --a first plurality of PMOSs-- and the second instance should read --a second plurality of PMOS--.

In claim 13, the phrase "a plurality of NMOSs" in line 6 should read --a first plurality of NMOSs-- and the phrase "NMOSs" in line 9 should read --a second plurality of NMOSs--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1, 2 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1, 2 and 6, in lines 3-4 it is not clear what is meant by the limitation, "a level shift core circuit which is controlled by a control circuit and/ or controls a pull-up and/ or pull-down circuit". Applicant needs to make clear which of the following components are optional and which are necessary: level shift core circuit, control circuit, pull-up, and pull-down. Furthermore, applicant needs to clarify what exactly is controlling the pull-up and/or pull-down circuit. When addressing the issue, applicant is asked to focus their attention on the first instance of "and/ or" in the recited limitation since it contributes mostly to the confusion.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 3 and 10 rejected under 35 U.S.C. 102(e) as being anticipated by Tsuji et al. (USP 6,373,315 B2).

Tsuji et al.'s Fig. 8 shows a level shift circuit for changing the signal level in a first logic circuit (1) fed from a first power supply (VDD) to the signal level in a second logic circuit (3) fed from a second power supply (VPP), including a level shift core circuit (6, 10, 11 and 27) which is controlled by a control circuit (21 and 22) that controls a pull-up circuit (transistor pairs 8, 5 and 28, 25), wherein:

the level shift core circuit, being fed from the second power supply, receives signals output from the first logic circuit and outputs signals to be input to the second logic circuit;

the control circuit includes: a NOR circuit (22) fed from the second power supply, which receives an inverted signal of the level shift input signals and a non-inverted signal of the level shift output signals; and a NOR circuit (21) fed from the second power supply, which receives a non-inverted signal of the level shift input signals and an inverted signal of the level shift output signals; and

the control circuit outputs the output signals of the two NOR circuits as control signals (they control pull-ups 8, 5 and 28, 25) as called for in claims 1 and 3.

Regarding claim 10, Tsuji et al.'s Fig. 8 shows the level shift circuits of claims 1 and 3, wherein the level shift core circuit comprises a PMOS cross-coupled latch including a plurality of PMOSs (6 and 27) and a differential NMOS switch including a plurality of NMOSs (10 and 11):

wherein the source of each PMOS is connected to the second power supply (VPP), the gate of each PMOS is connected to the level shift output through the drain of another PMOS (N6 and N7), the source of each NMOS of the differential NMOS switch is connected to the ground voltage GND, the drain of each NMOS is connected to the level shift output, and the gate of each NMOS is connected to the level shift input (Φ1 and Φ2).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuji et al.

Tsuji et al.'s Fig. 8 shows the level shift circuits as set forth above in claims 1 and 3.

Tsuji et al. does not show the NOR circuitry's PMOS transistors having the condition in which the polarity of the threshold is negative and the absolute value of the threshold voltage is large as called for in claim 5. However, it is notoriously well know to use a transistor with a large threshold voltage in order to reduce leakage current. Therefore, it would have been obvious to a person skilled in the art at the time the

invention was made to increase the absolute value of the threshold voltage of the PMOS transistors in Tsuji et al.'s NOR circuits for the purpose of reducing power consumption.

12. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuji et al. in view of applicant's prior art Fig. 2.

Tsuji et al.'s Fig. 8 shows the level shift circuits as set forth above in claims 1 and 3.

Tsuji et al. does not show a level shift core circuit with the configuration as called for in claim 12. Applicant's prior art Fig. 2 (same as Fig. 16) teaches this configuration for the benefit of weakening the cross bond between the PMOSs forming the PMOS cross-couple (pg. 19: 10-12). Therefore it would have been obvious to one skilled in the art at the time the invention was made to replace the level shift core circuit of Tsuji et al.'s invention (6, 10, 11 and 27) with applicant's prior art level shift core circuit (Fig. 2) for the purpose of accelerating the transition between high and low.

13. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuji et al. in view of applicant's prior art Fig. 3.

Tsuji et al.'s Fig. 8 shows the level shift circuits as set forth above in claims 1 and 3.

Tsuji et al. does not show a level shift core circuit with the configuration as called for in claim 13. Applicant's prior art Fig. 3 (same as Fig. 17) teaches this configuration for the benefit of performing a higher speed level shift (pg. 19: 27-30). Therefore it would have been obvious to one skilled in the art at the time the invention was made to

replace the level shift core circuit of Tsuji et al.'s invention (6, 10, 11 and 27) with applicant's prior art level shift core circuit (Fig. 3) for the purpose of faster level shifting and ensuring the margin of level shift operation when the potential difference between first and second power supplies increases.

14. Claims 2, 4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuji et al. (USP 6,373,315 B2) in view of Stopper (USP 3,828,202).

Tsuji et al.'s Fig. 8 shows the level shift circuits as set forth above in claims 1 and 3 which mostly read on claims 2 and 4, respectively.

Tsuji et al. does not show a plurality of inverters fed from the second power supply and receiving the outputs of the NOR circuits as called for in claims 2 and 4. Stopper teaches that it is advantageous to work with logic circuits that perform direct logical functions, i.e., AND and OR, rather than complementary logical functions, i.e., NAND and NOR in order to facilitate the design process (col. 1: 56-60). Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to add inverters to the outputs of Tsuji et al.'s NOR circuits, converting them to OR circuits as per the teachings of Stopper, for the purpose of ease of design and visualization.

Regarding claim 10, the combination of Tsuji et al. and Stopper shows the level shift circuits of claims 2 and 4, wherein the level shift core circuit comprises a PMOS cross-coupled latch including a plurality of PMOSs (6 and 27; Tsuji et al. Fig. 8) and a differential NMOS switch including a plurality of NMOSs (10 and 11):

wherein the source of each PMOS is connected to the second power supply (VPP), the gate of each PMOS is connected to the level shift output through the drain of another PMOS (N6 and N7), the source of each NMOS of the differential NMOS switch is connected to the ground voltage GND, the drain of each NMOS is connected to the level shift output, and the gate of each NMOS is connected to the level shift input (Φ1 and Φ2).

15. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuji et al. and Stopper as applied to claims 2 and 4 above, and further in view of applicant's prior art Fig. 2.

The combination of Tsuji et al. and Stopper does not show a level shift core circuit with the configuration as called for in claim 12. Applicant's prior art Fig. 2 (same as Fig. 16) teaches this configuration for the benefit of weakening the cross bond between the PMOSs forming the PMOS cross-couple (pg. 19: 10-12). Therefore it would have been obvious to one skilled in the art at the time the invention was made to replace the level shift core circuit of the combination of Tsuji et al. and Stopper (6, 10, 11 and 27; Tsuji et al. Fig. 8) with applicant's prior art level shift core circuit (Fig. 2) for the purpose of accelerating the transition between high and low.

16. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuji et al. and Stopper as applied to claims 2 and 4 above, and further in view of applicant's prior art Fig. 3.

The combination of Tsuji et al. and Stopper does not show a level shift core circuit with the configuration as called for in claim 13. Applicant's prior art Fig. 3 (same

as Fig. 17) teaches this configuration for the benefit of performing a higher speed level shift (pg. 19: 27-30). Therefore it would have been obvious to one skilled in the art at the time the invention was made to replace the level shift core circuit of the combination of Tsuji et al. and Stopper (6, 10, 11 and 27; Tsuji et al. Fig. 8) with applicant's prior art level shift core circuit (Fig. 3) for the purpose of faster level shifting and ensuring the margin of level shift operation when the potential difference between first and second power supplies increases.

17. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Tsuji et al. and Stopper.

The combination of Tsuji et al and Stopper shows the level shift circuits as set forth above in claims 2 and 4.

The combination of Tsuji et al. and Stopper does not show the NOR circuitry's PMOS transistors having the condition in which the polarity of the threshold is negative and the absolute value of the threshold voltage is large as called for in claim 5. However, it is notoriously well know to use a transistor with a large threshold voltage in order to reduce leakage current. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to increase the absolute value of the threshold voltage of the PMOS transistors in the combination of Tsuji et al. and Stopper's NOR circuits for the purpose of reducing power consumption.

18. Claims 6, 7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuji et al. in view of Yang (USP 6,388,602).

Tsuji et al.'s Fig. 8 shows the level shift circuits as set forth above in claims 1 and 3 which mostly read on claims 6 and 7, respectively.

Tsuji et al. does not show a control circuit made up of NAND circuits as called for in claims 6 and 7. Yang teaches that NAND gate operation has the advantage of being faster than OR or NOR gate operation in some of the logic families, especially in CMOS logic (col. 6: 17-23). Therefore it would have been obvious to one skilled in the art at the time the invention was made to replace the NOR circuits in the combination of Tsuji et al. and Stopper with NAND circuits -in the process, reversing all polarities and transistor conductivity types in order to maintain functionality- as per the teachings of Yang for the purpose of faster speed.

Regarding claim 10, the combination of Tsuji et al. and Yang shows the level shift circuits of claims 6 and 7, wherein the level shift core circuit comprises a PMOS cross-coupled latch including a plurality of PMOSs (6 and 27; Tsuji et al. Fig. 8) and a differential NMOS switch including a plurality of NMOSs (10 and 11):

wherein the source of each PMOS is connected to the second power supply (VPP), the gate of each PMOS is connected to the level shift output through the drain of another PMOS (N6 and N7), the source of each NMOS of the differential NMOS switch is connected to the ground voltage GND, the drain of each NMOS is connected to the level shift output, and the gate of each NMOS is connected to the level shift input ($\Phi 1$ and $\Phi 2$).

19. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuji et al. and Yang as applied to claims 6 and 7 above, and further in view of applicant's prior art Fig. 2.

The combination of Tsuji et al. and Yang does not show a level shift core circuit with the configuration as called for in claim 12. Applicant's prior art Fig. 2 (same as Fig. 16) teaches this configuration for the benefit of weakening the cross bond between the PMOSs forming the PMOS cross-couple (pg. 19: 10-12). Therefore it would have been obvious to one skilled in the art at the time the invention was made to replace the level shift core circuit of the combination of Tsuji et al. and Yang (6, 10, 11 and 27; Tsuji et al. Fig. 8) with applicant's prior art level shift core circuit (Fig. 2) for the purpose of accelerating the transition between high and low.

20. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuji et al. and Yang as applied to claims 6 and 7 above, and further in view of applicant's prior art Fig. 3.

The combination of Tsuji et al. and Yang does not show a level shift core circuit with the configuration as called for in claim 13. Applicant's prior art Fig. 3 (same as Fig. 17) teaches this configuration for the benefit of performing a higher speed level shift (pg. 19: 27-30). Therefore it would have been obvious to one skilled in the art at the time the invention was made to replace the level shift core circuit of the combination of Tsuji et al. and Yang (6, 10, 11 and 27; Tsuji et al. Fig. 8) with applicant's prior art level shift core circuit (Fig. 3) for the purpose of faster level shifting and ensuring the margin of

level shift operation when the potential difference between first and second power supplies increases.

21. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Tsuji et al. and Yang.

The combination of Tsuji et al. and Yang shows the level shift circuit as set forth above in claims 6 and 7.

The combination of Tsuji et al. and Yang does not show the NAND circuitry's PMOS transistors having the condition in which the polarity of the threshold is negative and the absolute value of the threshold voltage is large as called for in claim 9. However, it is notoriously well know to use a transistor with a large threshold voltage in order to reduce leakage current. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to increase the absolute value of the threshold voltage of the PMOS transistors in the combination of Tsuji et al. and Yang's NAND circuits for the purpose of reducing power consumption.

22. Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Tsuji et al. and Stopper as applied to claim 4 above, and further in view of Yang.

The combination of Tsuji et al. and Stopper shows the level shift circuits as set forth above in claim 4 which mostly reads on claim 8 as well.

The combination of Tsuji et al. and Stopper does not show a control circuit made up of NAND circuits as called for in claim 8. Yang teaches that NAND gate operation has the advantage of being faster than OR or NOR gate operation in some of the logic

families, especially in CMOS logic (col. 6: 17-23). Therefore it would have been obvious to one skilled in the art at the time the invention was made to replace the NOR circuits in the combination of Tsuji et al. and Stopper with NAND circuits -in the process, reversing all polarities and transistor conductivity types in order to maintain functionality- as per the teachings of Yang for the purpose of faster speed.

Regarding claim 10, the combination of Tsuji et al., Stopper and Yang shows the level shift circuit of claim 8, wherein the level shift core circuit comprises a PMOS cross-coupled latch including a plurality of PMOSs (6 and 27; Tsuji et al. Fig. 8) and a differential NMOS switch including a plurality of NMOSs (10 and 11):

wherein the source of each PMOS is connected to the second power supply (VPP), the gate of each PMOS is connected to the level shift output through the drain of another PMOS (N6 and N7), the source of each NMOS of the differential NMOS switch is connected to the ground voltage GND, the drain of each NMOS is connected to the level shift output, and the gate of each NMOS is connected to the level shift input (Φ1 and Φ2).

23. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuji et al., Stopper and Yang as applied to claim 8 above, and further in view of applicant's prior art Fig. 2.

The combination of Tsuji et al., Stopper and Yang does not show a level shift core circuit with the configuration as called for in claim 12. Applicant's prior art Fig. 2 (same as Fig. 16) teaches this configuration for the benefit of weakening the cross bond between the PMOSs forming the PMOS cross-couple (pg. 19: 10-12). Therefore it

would have been obvious to one skilled in the art at the time the invention was made to replace the level shift core circuit of the combination of Tsuji et al., Stopper and Yang (6, 10, 11 and 27; Tsuji et al. Fig. 8) with applicant's prior art level shift core circuit (Fig. 2) for the purpose of accelerating the transition between high and low.

24. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuji et al., Stopper and Yang as applied to claim 8 above, and further in view of applicant's prior art Fig. 3.

The combination of Tsuji et al., Stopper and Yang does not show a level shift core circuit with the configuration as called for in claim 13. Applicant's prior art Fig. 3 (same as Fig. 17) teaches this configuration for the benefit of performing a higher speed level shift (pg. 19: 27-30). Therefore it would have been obvious to one skilled in the art at the time the invention was made to replace the level shift core circuit of the combination of Tsuji et al., Stopper and Yang (6, 10, 11 and 27; Tsuji et al. Fig. 8) with applicant's prior art level shift core circuit (Fig. 3) for the purpose of faster level shifting and ensuring the margin of level shift operation when the potential difference between first and second power supplies increases.

25. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Tsuji et al., Stopper and Yang.

The combination of Tsuji et al., Stopper and Yang shows the level shift circuit as set forth above in claim 8.

The combination of Tsuji et al., Stopper and Yang does not show the NAND circuitry's PMOS transistors having the condition in which the polarity of the threshold is

negative and the absolute value of the threshold voltage is large as called for in claim 9. However, it is notoriously well know to use a transistor with a large threshold voltage in order to reduce leakage current. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to increase the absolute value of the threshold voltage of the PMOS transistors in the combination of Tsuji et al., Stopper and Yang's NAND circuits for the purpose of reducing power consumption.

Allowable Subject Matter

26. Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bismarck (USP 4,450,371 and 4,532,436) are cited to teach level shift circuits that output to NOR/NAND circuits which in turn control pull-up circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Hernandez whose telephone number is (571) 272-8979. The examiner can normally be reached on Mon.-Fri. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

WH

WH 8/18/06

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